Linear X-Ray Photodiode Detector Array with Signal Amplification

XB90802 TDI Series

An X-Scan Imaging XB90802 TDI linear detector array is constructed of CMOS silicon photodiode array detector chips mounted on a single printed-circuit board. The imaging circuit of each detector chip consists of 8- row contiguous linear arrays of photodiodes, a timing generator, digital scanning shift register, an array of charge integrating amplifiers, sample-and-hold circuits, and signal amplification chain. Each detector array generates an End-Of-Scan (EOS) pulse that can be used to initiate the scanning of the next detector array. Thus, a longer, continuous detector array can be formed from a daisy chain of smaller detector arrays.

For x-ray scanning applications, a scintillator material tailored to the user's application is attached to the surface of the detector array to convert x-ray photons into visible light for detection by the photodiode array. The XB90802 photodiode arrays are uniquely designed and processed to reduce radiation damage from the x-ray flux. The signal processing circuits are positioned 2 mm away from the photodiode array. These circuits are shielded from direct x-ray radiation using an external heavy-metal shield. The precision alignment of the metal shield with respect to the signal processing circuits is performed at the factory using a special molded housing and chip-on-board (COB) technology.

Key Features

- Element pitch resolution of 0.2 mm with 8 TDI stages
- 2-inch sensor board length with 256 sensitive pixels
- 6, 8, and 10-inch continuous butt-able sensor board options
- 1 dark reference pixel for every 64 sensitive pixels
- 5-V power supply operation
- Simultaneous integration by using an array of charge integrating amplifiers
- Sequential readout with a digital scanning shift register (Data rate: 2 MHz max.)
- Integrated CDS circuits allow low noise and wide dynamic range up to > 3000
- User-specified scintillator material options

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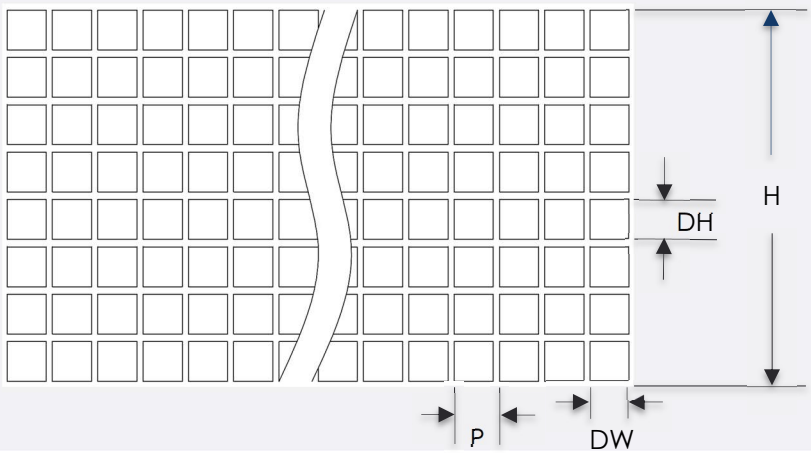
Applications

Food and industrial inspection
Package content inspection
Security and cargo screening
Industrial non-destructive testing (NDT)

Mechanical specifications

Parameter	Symbol[1]	XB90802-2.0[2]	XB90802-8.0[3]	XB90802-10.0[4]	Unit
Element pitch (Vertical and Horizontal)	P	0.200	0.200	0.200	mm
Element diffusion width	DW	0.166	0.166	0.166	mm
Element diffusion height	DH	0.166	0.166	0.166	mm
Element height	H	0.200 X 8 stages	0.200 X 8 stages	0.200 X 8 stages	mm
Number of active pixels	-	256	1024	1280	-
Active area length	-	51.2	204.8	256	mm
Number of TDI Stages	-	8	8	8	-

Enlarged view of active area



[1] Refer to enlarged view of active area figure.
[2] 2-inch long detector is specified here.
[3] 8-inch long detector is specified here.
[4] 10-inch long detector is specified here.
Other lengths (at multiples of 0.5 inches) are available upon request.

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Absolute maximum ratings

Electronic device is sensitive to electrostatic discharge and x-ray radiation. Although this device features ESD protection circuitry, permanent damage ranging from subtle performance degradation to complete device failure may occur on devices subjected to high-energy electrostatic discharges. Furthermore, although this device features radiation shielding for protection against anticipated x-ray radiation, permanent damage ranging from subtle performance degradation to complete device failure may occur on devices subjected to unanticipated x-ray radiation (e.g. off-axis or extremely high energy radiation). Therefore, proper precautions against ESD and x-ray radiation must be taken during handling and storage of this device.

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	-0.3	+6	V
Reference voltage	VREF	-0.3	VDD + 0.3	V
Digital input voltages		-0.3	VDD + 0.3	V
Operating temperature[5]	Topr	-5	+60	°C
Storage temperature	Tstg	-10	+70	°C

Recommended terminal voltage

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage[6]	VDD	4.90	5	5.35	V
Reference voltage	VREF[7]	-	4.2	4.5	V

[5] Humidity must be controlled to prevent the occurrence of condensation.
[6] Both VDD and Vref have direct influence on the output video signal. For a clean video signal, it is advised that VDD and Vref have a stability that is commensurate with the noise level desired.
[7] VREF 4.2 is recommended. Reduction of VREF will reduce dynamic range.

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Electrical characteristics [Ta = 21°C, VDD = 5V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital						
Clock pulse frequency[8]		f(CLK)	40	–	8000	kHz
Digital input voltage[9]	High level	Vih	VDD-1.00	VDD	VDD	V
	Low level	Vil	0	0	0.4	V
Digital input capacitance		Ci	–	40	–	pF
Digital input leakage current		Ii	-10	10	–	μA
Digital output voltage[10]	High level	Voh	VDD-0.75	VDD	VDD	V
	Low level	Vol	0	0	0.4	V
Digital output load capacitance		Co	–	–	<35	pF
Analog						
Reference voltage input impedance[11]		Rref	–	3.0	–	kΩ
Charge amplifier feedback cap	High sensitivity	Cfhs		1		pF
	Low sensitivity	Cfls		1.6		pF
Video output impedance		Zv	–	1	–	kΩ
Video output load capacitance		Cv	–	–	100	pF
Power						
Power consumption		P	–	850	–	mW

[8] Video rate is 1/4 of clock pulse frequency f (CLK).
[9] Digital inputs include CLK, RESET, EXTSP, VMS, SNS, and RS (see pin connections).
[10] Digital outputs include Trig and EOS (see pin connections).
[11] Reference voltage input impedance is dependent on length of detector. For a 2-inch detector (XB90802-2.0), the input impedance is 3 kΩ.

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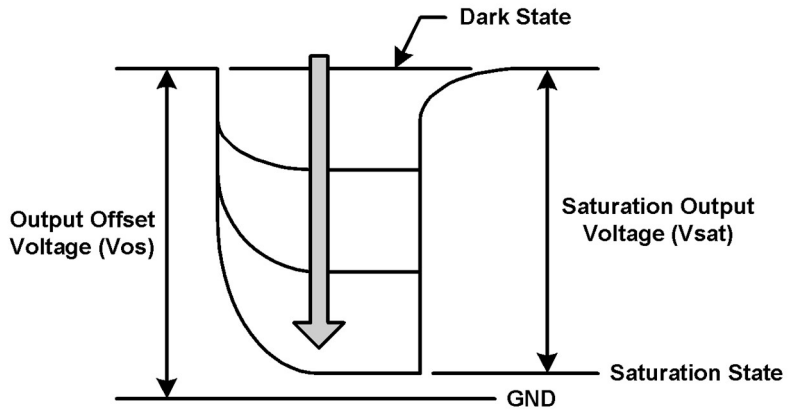
Output waveform of one element



Radio-opto-electrical characteristics [Ta = 21°C, VDD = 5 V, V(SNS) = 5 V (High sensitivity), 0 V (Low sensitivity)]

Parameter		Symbol	XB90802 (0.2 mm)			Unit
			Min.	Typ.	Max.	
Output offset voltage[12]		Vos	–	VREF	–	V
Dark offset voltage[13]	High Sensitivity	Vd	-150	–	450	mV
	Low Sensitivity		--200		450	
X-ray sensitivity[14]	High Sensitivity	S	–	2.6M	–	V/Gy
	Low Sensitivity		–	1.7M	–	
Photo response non-uniformity[15]		PRNU	-15	–	10	%
Noise[16]	High Sensitivity	N	–	3.8	–	mVrms
	Low Sensitivity		–	3.6	–	
Saturation output voltage		Vsat	2.5	-	-	V

[12] Video output is negative-going output with respect to the output offset voltage.
[13] Difference between output signal under dark conditions and Vref with an integration time of 1 ms.
[14] Measured with tube energy of 70kVp. Other scintillations with different sensitivity are available.
[15] Measured without scintillation. When the photodiode array is exposed to uniform light which is 50% of the saturation exposure, the Photo Response Non Uniformity (PRNU) is defined as follows:

$$PRNU = \Delta X \div X \times 100\%$$

where X is the average output of all elements and ΔX is the difference between the maximum and minimum outputs.
[16] Measured with a video data rate of 750 kHz and an integration time of 1 ms in dark state.

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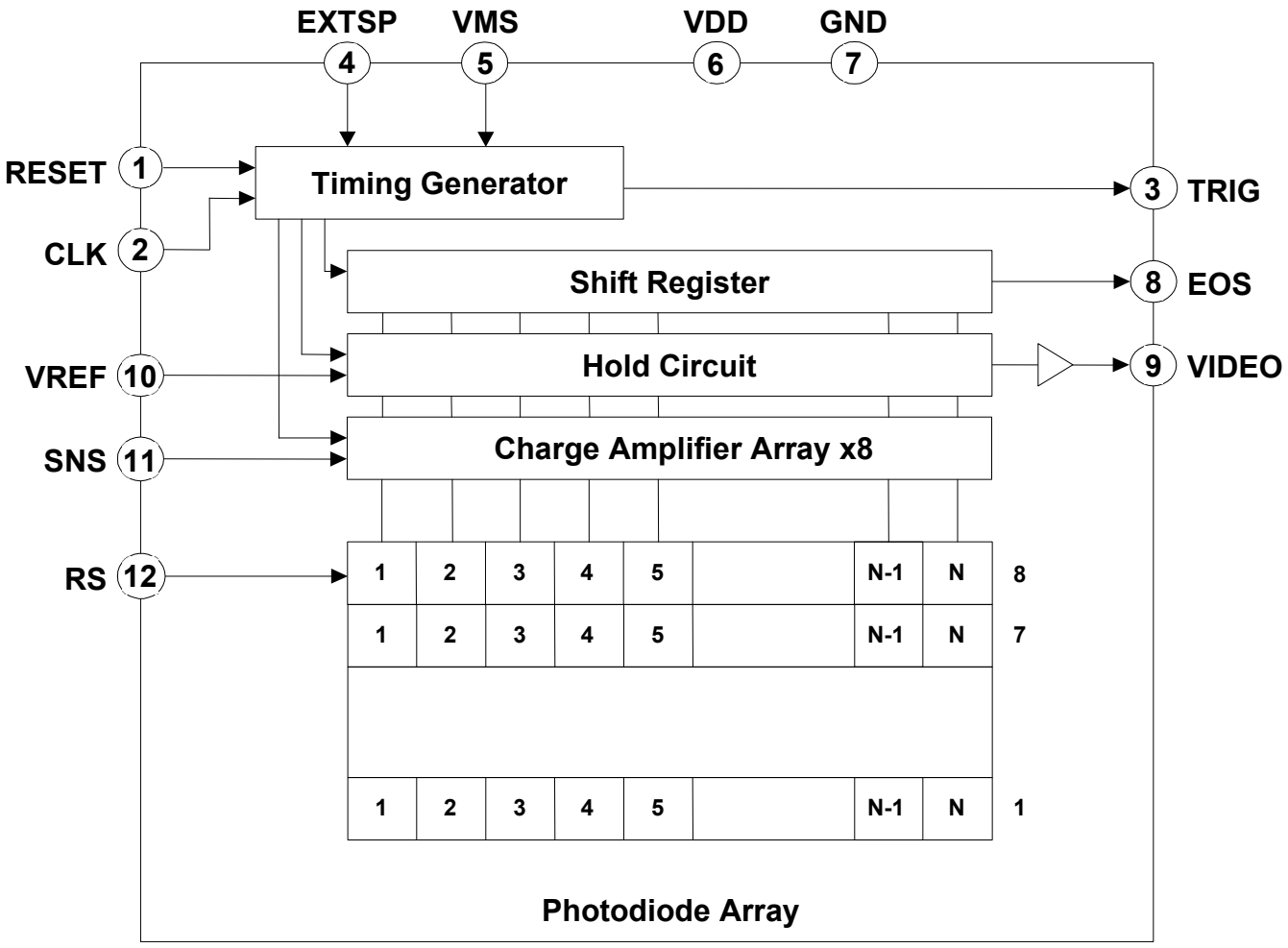
Block diagram



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Pin connections

Pin No.	Symbol	Name	Description
1	RESET	Reset Pulse	Negative-going pulse input
2	CLK	Clock Pulse	Pulse input
3	TRIG	Trigger Pulse	Positive-going pulse output
4	EXTSP	External Start Pulse	Pulse/voltage input
5	VMS	Master/Slave Selection	Voltage input: See Master/slave selection voltage VMS and external start pulse EXTSP settings note
6	VDD	Supply Voltage	5-V supply voltage
7	GND	Ground	Common ground voltage
8	EOS	End of Scan	Negative-going pulse output
9	VIDEO	Video Output	Negative-going output with respect to VREF
10	VREF	Reference Voltage	Voltage input
11	SNS	Sensitivity Selection	Voltage input: High (VDD) for high sensitivity (Cfhs) Low (GND) for low sensitivity (Cfls)
12	NC	No Connection	Disabled

Readout circuit

In order to minimize noise and to maximize performance, an operational amplifier should be placed as close to the detector as possible to amplify the Video signal.

Master/slave selection voltage VMS and external start pulse EXTSP Settings

For most applications, multiple detectors are read out in parallel. To ensure parallel read out, set the VMS input of all detectors to VDD (A in the table below).

In applications where two or more linearly connected detectors are read out sequentially (in series), set the VMS input of the first detector to VDD and the VMS input of each subsequent (second and later) detector to GND while connecting the EXTSP input of each subsequent detector to the EOS output of each respective preceding detector (B in the table below). The CLK and RESET pulses should be shared among all detectors and the Video output terminals of all detectors are connected together. The maximum number of detectors that can be daisy-chained together is limited by the maximum Video output capacitance requirement.

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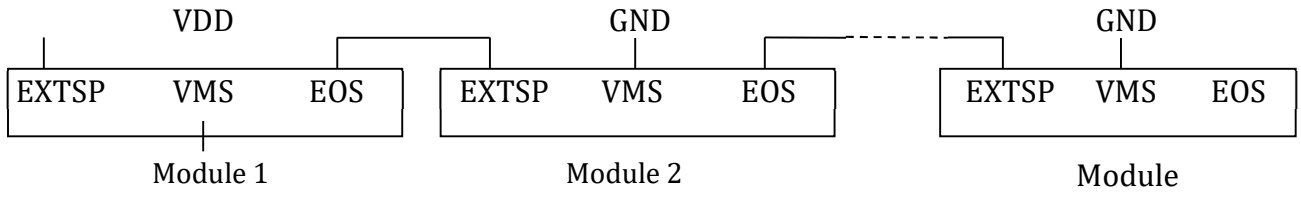
Master/slave selection voltage VMS and external start pulse EXTSP Settings

	Operation Mode	VMS	EXTSP
A	Master configuration: Parallel readout: all detectors Serial readout: 1st detector only	VDD	Not Applicable
B	Slave configuration: Serial readout: 2nd and later detectors	GND	Preceding detector's EOS should be input

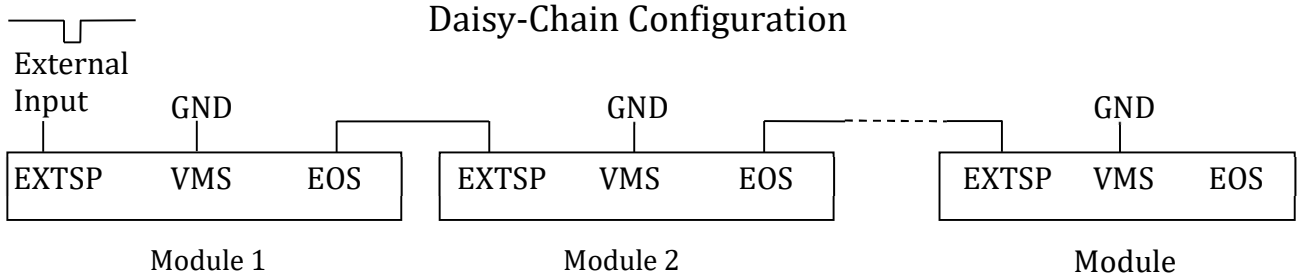
Daisy-Chain Configuration

Our modules can be daisy-chained. The following diagram is an example of a daisy-chained array of modules with both master-mode and slave-mode configurations. In the master mode, the first module's VMS input is connected to VDD. In the slave mode, the first module's VMS is connected to GND and the EXTSP input requires a negative pulse. Each individual subsequent module is configured in slave mode. Each slave module must have its EXTSP input connected to the preceding module's EOS output.

Master-Mode
Daisy-Chain Configuration



Slave-Mode
Daisy-Chain Configuration



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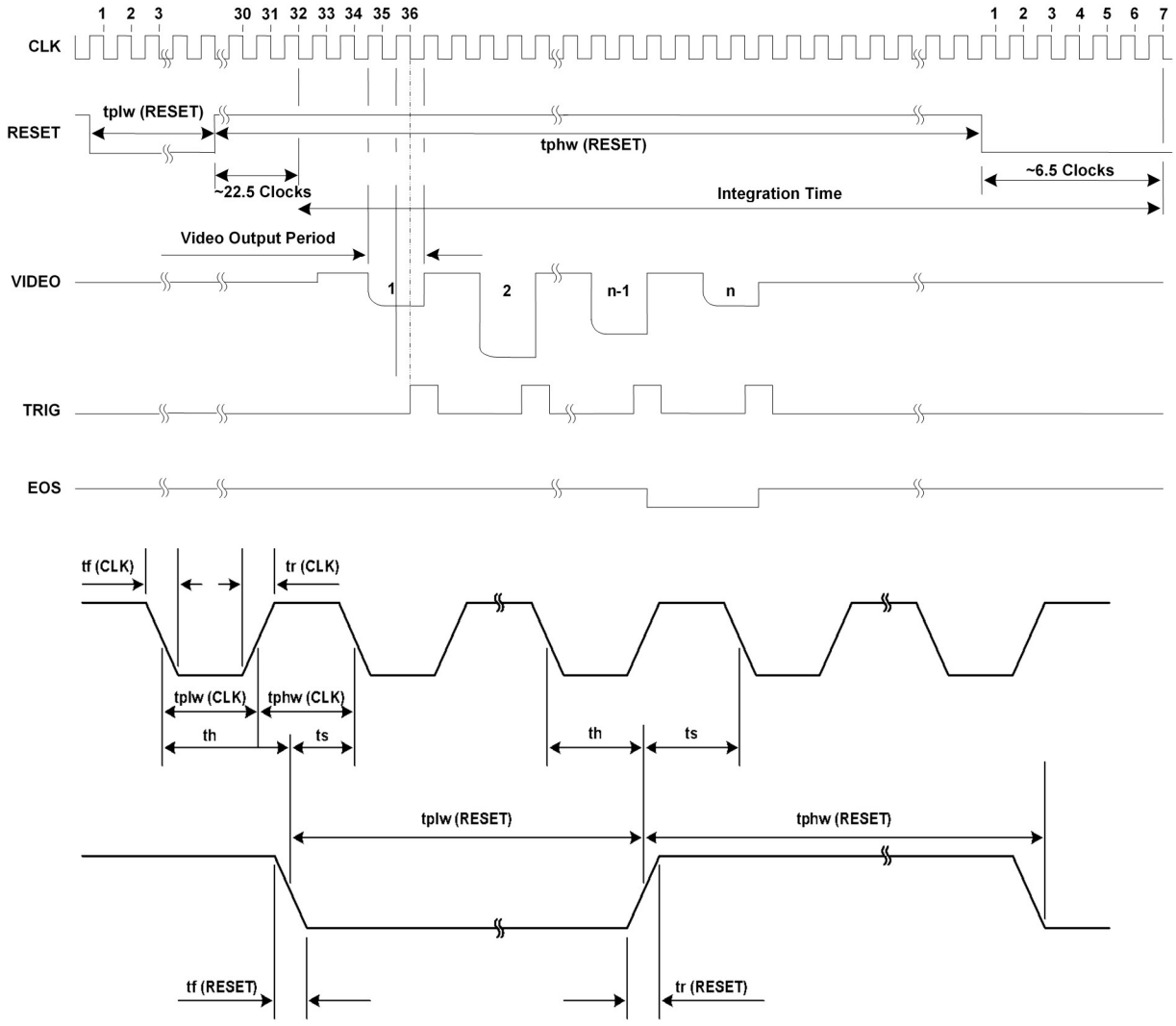
Master mode timing chart [xvi]



[xvi] The falling of Video just before the 19th falling edge of CLK after transition of RESET from High to Low corresponds to the first pixel. The video output for the first pixel should be read around the 20th falling edge and before the subsequent rising CLK edge while Trig is high. After the first pixel, a pixel output appears on Video at every 4th clock cycle.

Care should be taken to prevent the rising edge of the RESET during the video output. Improper positioning of the RESET edges can lead to interference with the read-out. The falling edge of the RESET should follow the last pixel of the previous line's read-out. Thus, one cycle of RESET pulses cannot be set shorter than the time equal to (38 + 4 × N) clock cycles, where N is the number of pixels.

EOS of each detector chip appears during the output of the last pixel.

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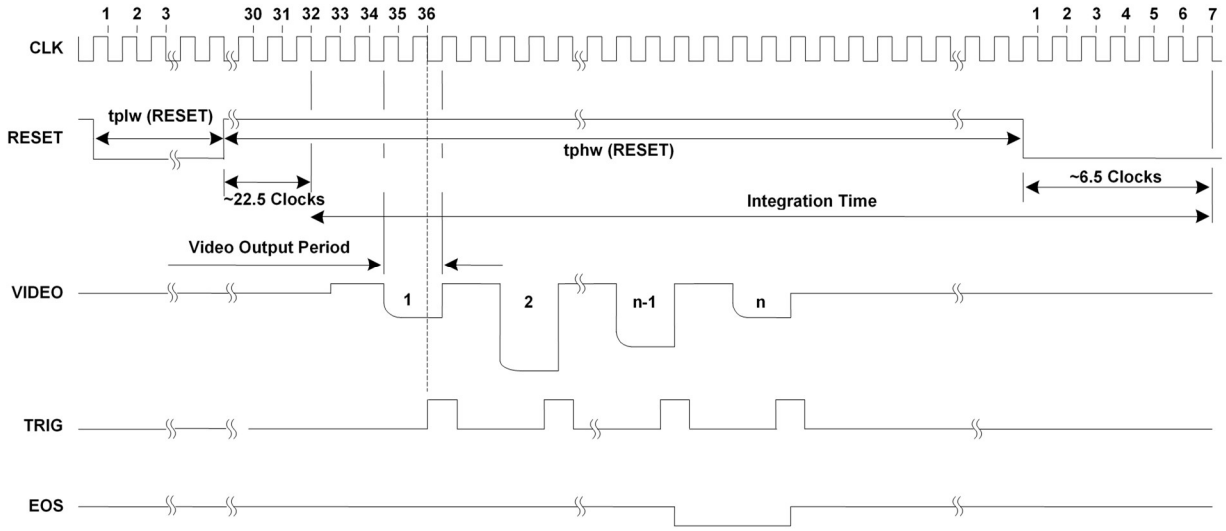
Master mode timing chart

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse low/high width	tplw (CLK), tphw (CLK)	40	62.5	–	ns
Clock pulse rise/fall times	tr (CLK), tf (CLK)	0	15	20	ns
Reset pulse low width[17]	tplw (RESET)	12 / f(CLK)	16 / f(CLK)	–	ms
Reset pulse high width[18]	tphw (RESET)	20	–	–	µs
Reset pulse rise/fall times	tr (RESET), tf (RESET)	0	15	20	ns
Reset pulse setup time[19]	ts	20	–	–	ns
Reset pulse hold time	th	20	–	–	ns

Slave mode timing chart

In the slave mode (VMS=GND), the video will start 4 clock periods after the falling edge of EXTSP. The EXTSP negative pulse duration should be longer than 3 clock periods and no more than 5 clock periods. The EXTSP's falling edge should come at least 24 clock periods after RESET's rising edge. Please refer to below picture for detail timing.



[17] RESET must stay Low [tplw(RESET)] for at least twelve clock cycles.

[18] The falling edge of RESET pulse determines the end of the integration time and the start of signal read-out, while the rising edge of the RESET pulse determines the start of the integration time. As a result, the signal-charge integration time can be controlled externally with the width of the RESET pulse [tphw(RESET)]. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th falling edge of clock after the rise of the RESET pulse and ends at the 7th falling edge of clock after the fall of the RESET pulse.

[19] The rising and falling edges of RESET must observe the setup and hold time requirements around the falling edges of CLK.

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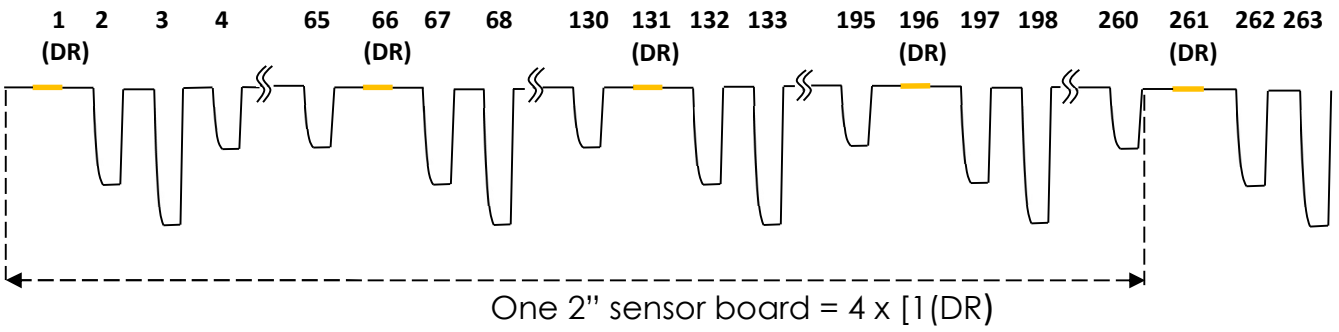
Dark reference pixels

The locations of the dark reference (DR) pixels are shown in orange:



The "zero" pixels are dark reference pixels. For every 64 responsive pixels, there is one additional dark reference pixel. On a single card, we output 256 responsive pixels and 4 dark reference pixels for a total of 260 pixels. The dark reference pixels are sensitive to temperature, as are the responsive pixels when no radiation is present. So, the intent is to use the dark reference pixels to compensate for temperature variations.

On the timing diagrams on pages 8 and 9, the VIDEO output has 1 through n pixels where n = 260 for one card. The dark reference pixels are 1, 66, 131, and 196. The responsive pixels are 2-65, 67-130, 132-195, and 197-260.

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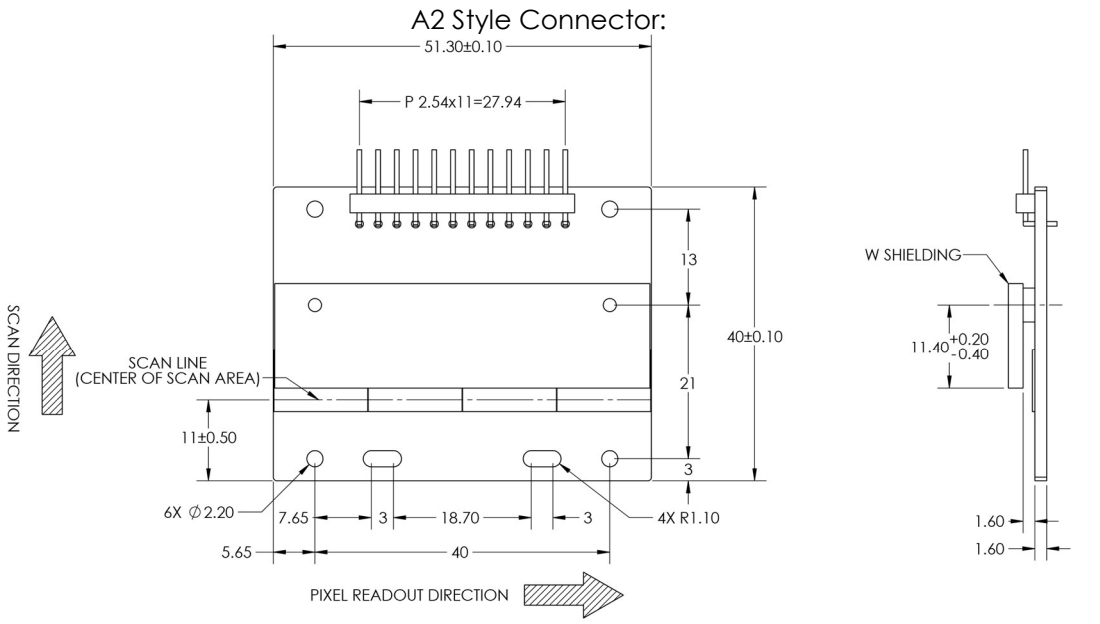
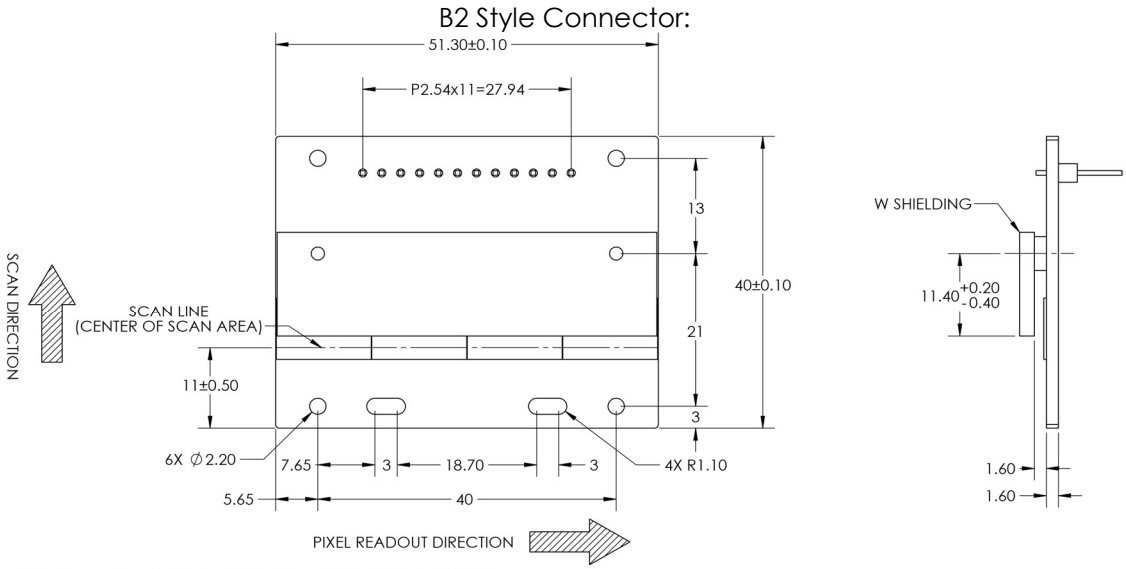
Mechanical drawings [xx]

2-inch (51.2mm) Sensor Boards



NOTE: ALL W SHIELDING ARE 3MM THICK.



NOTE: ALL W SHIELDING ARE 3MM THICK.

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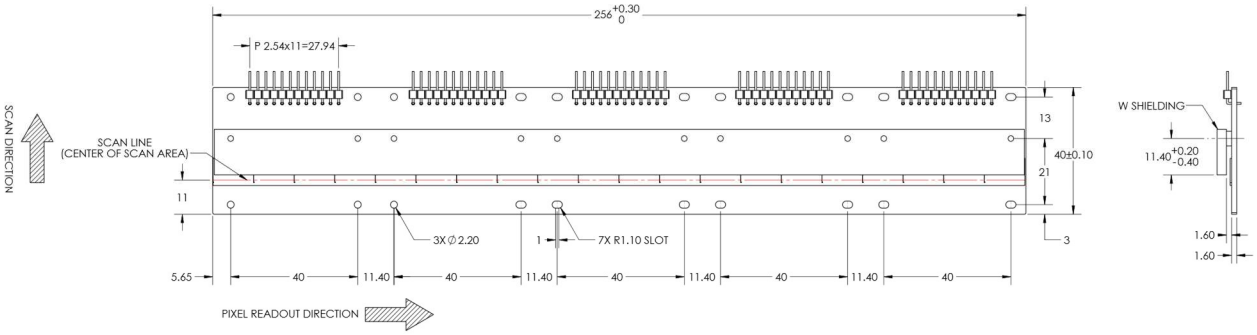
Mechanical drawings [xx]

10-inch (256mm) sensor board

A2 Style Connector shown, B2 also available:



NOTE: ALL W SHIELDING ARE 3MM THICK.

[xx] Unit: Dimensions are in millimeters (mm).
Board: FR4 epoxy resin bonded glass fabric.
Connector: BISON Advanced Technology Corp., Ltd. (www.bison-protech.com), P101-RGP-060/030-12 or similar.

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