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Linear X-Ray Photodiode Detector Array with Signal Amplification

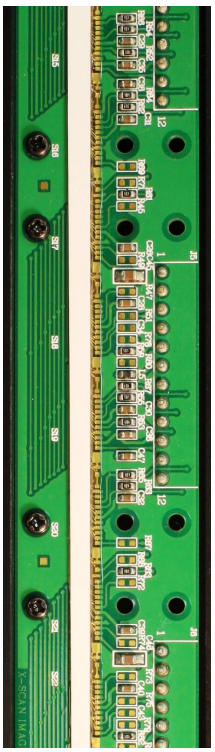
XB8850 Series

An X-Scan Imaging XB8850 linear detector array is constructed of CMOS silicon photodiode array detector chips mounted on a single printed-circuit board. The imaging circuit of each detector chip consists of a contiguous linear array of photodiodes, a timing generator, digital scanning shift register, an array of charge integrating amplifiers, sample-and-hold circuits, and signal amplification chain. Each detector array generates an End-Of-Scan (EOS) pulse that can be used to initiate the scanning of the next detector array. Thus, a longer, continuous detector array can be formed from a daisy chain of smaller detector arrays.

For x-ray scanning applications, a scintillator material tailored to the user's application is attached to the surface of the detector array to convert x-ray photons into visible light for detection by the photodiode array. The XB8850 photodiode array is uniquely designed and processed to reduce radiation damage from the x-ray flux. The signal processing circuits are positioned 2 mm away from the photodiode array. These circuits are shielded from direct x-ray radiation using an external heavy-metal shield. The precision alignment of the metal shield with respect to the signal processing circuits is performed at the factory using a special molded housing and chip-on-board (COB) technology.

Key Features

- Small element pitch with two selectable resolution modes: 50 µm and 100 µm
- A large selection of lengths at multiples of 0.5 inches:
  - 0.5 inches (256 pixels at 50 µm, 128 pixels at 100 µm)
  - 1.0 inch (512 pixels at 50 µm, 256 pixels at 100 µm)
  - 1.5 inches (768 pixels at 50 µm, 384 pixels at 100 µm)
  - 2.0 inches (1024 pixels at 50 µm, 512 pixels at 100 µm)
  - etc.
- 5-V power supply operation
- Simultaneous integration by using an array of charge integrating amplifiers
- Sequential readout with a digital scanning shift register (Data rate: 1 MHz max.)
- Integrated CDS circuits allow low noise and wide dynamic range up to > 4000
- User-specified scintillator material GOS, CsI(Tl), $CdWO_4$, etc.



Applications

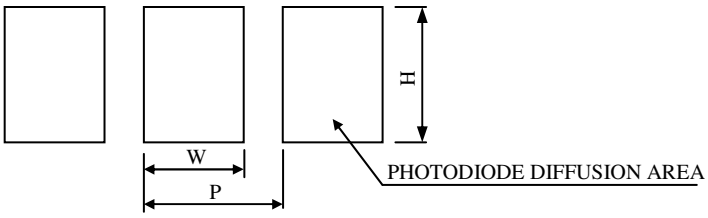
- Linear x-ray imaging for industrial inspection
- Linear x-ray imaging for biological and industrial CT

■ Mechanical specifications

Parameter	Symbol[i]	XB8850-6.0G[ii]		XB8850-12.0G[iii]		Unit
		100 µm[iv]	50 um[v]	100 µm[iv]	50 um[v]	
Element pitch	P	100	50	100	50	µm
Element diffusion width	W	40×2	40	40×2	40	µm
Element height	H	75	75	75	75	µm
Number of elements	–	1536	3072	3072	6144	–
Active area length	–	153.6	153.6	307.2	307.2	mm

[i] Refer to enlarged view of active area figure.
[ii] 6-inch long detector is specified here. Other lengths (at multiples of 0.5 inches) are available upon request.
[iii] 12-inch long detector is specified here. Other lengths (at multiples of 0.5 inches) are available upon request.
[iv] When RS (pin 12) is tied to GND, the detector operates in the 100-µm resolution mode. There are 1536 pixels in a 6-inch 100-µm detector; there are 3072 pixels in a 12-inch 100-µm detector.
[v] When RS (pin 12) is tied to VDD, the detector operates in the 50-µm resolution mode. There are 3072 pixels in a 6-inch 50-µm detector; there are 6144 pixels in a 12-inch 50-µm detector.

■ Enlarged view of active area



■ Absolute maximum ratings

Electronic device sensitive to electrostatic discharge and x-ray radiation. Although this device features ESD protection circuitry, permanent damage ranging from subtle performance degradation to complete device failure may occur on devices subjected to high-energy electrostatic discharges. Furthermore, although this device features radiation shielding for protection against anticipated x-ray radiation, permanent damage ranging from subtle performance degradation to complete device failure may occur on devices subjected to unanticipated x-ray radiation (e.g. off-axis or extremely high energy radiation). Therefore, proper precautions against ESD and x-ray radiation must be taken during handling and storage of this device.

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	–0.3	+6	V
Reference voltage	VREF	–0.3	VDD + 0.3	V
Digital input voltages		–0.3	VDD + 0.3	V
Operating temperature[vi]	Topr	–5	+60	°C
Storage temperature	Tstg	–10	+70	°C

[vi] Humidity must be controlled to prevent the occurrence of condensation.

■ Recommended terminal voltage

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	4.75	5	5.25	V
Reference voltage	VREF	–	3.00	–	V

■ Electrical characteristics [Ta = 21°C, VDD = 5 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital						
Clock pulse frequency[vii]		f(CLK)	40	–	4000	KHz
Digital input voltage[viii]	High level	Vih	4.0	VDD	VDD	V
	Low level	Vil	0	0	0.4	V
Digital input capacitance		Ci	–	40	–	pF
Digital input leakage current		Ii	–10	+10	–	μA
Digital output voltage[ix]	High level	Voh	4.25	VDD	VDD	V
	Low level	Vol	0	0	0.4	V
Digital output load capacitance		Co	–	–	50	pF
Analog						
Reference voltage input impedance[x]	6.0G	Rref	–	1	–	KΩ
	12.0G		–	0.5	–	KΩ
Charge amplifier feedback capacitance[xi]	High sensitivity	Cfhs	–	0.1	–	pF
	Low sensitivity	Cfls	–	0.4	–	pF
Video output impedance		Zv	–	1	–	KΩ
Video output load capacitance		Cv	–	–	100	pF
Power						
Power consumption	6.0G	P	–	600	–	mW
	12.0G		–	1200	–	mW

[vii] Video rate is 1/4 of clock pulse frequency f(CLK).
[viii] Digital inputs include CLK, RESET, EXTSP, VMS, SNS, and RS (see pin connections).
[ix] Digital outputs include Trig and EOS (see pin connections).
[x] Reference voltage input impedance is dependent on length of detector. For a 6-inch detector (XB8850-6.0G), the input impedance is 1 KΩ. For a 12-inch detector (XB8850-12.0G), the input impedance is 0.5 KΩ.
[xi] The sensitivity selection pin (see SNS in pin connections) controls the sensitivity of the detector by selecting whether the pixel charge amplifier feedback capacitance is Cfhs or Cfls. At Cfhs, the detector has high sensitivity. At Cfls, the detector has low sensitivity.

■ **Electro-optical characteristics [Ta = 21°C, VDD = 5 V, V(SNS) = 5 V (High sensitivity), 0 V (Low sensitivity)]**

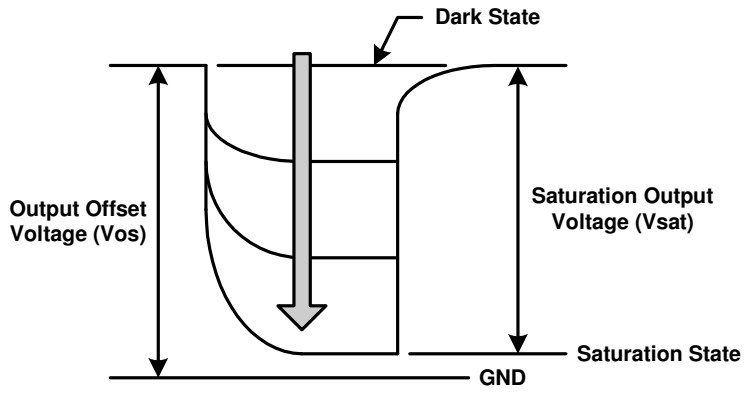
Parameter		Symbol	XB8850-6.0 /12.0 (100 um mode)			XB8850-6.0/12.0 (50 um mode)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output reference voltage[xii]		Vos	–	VREF	–	–	VREF	–	V
Dark signal voltage[xiii]	High sensitivity	Vd	–70	–	160	–90	–	70	mV
	Low sensitivity		–90	–	70	–100	–	70	
X-ray sensitivity[xiv]	High sensitivity	S	–	200	–	–	100	–	V/R
	Low sensitivity		–	50	–	–	25	–	
Photo response non-uniformity[xv]		PRNU	–10	–	10	–10	–	10	%
Noise[xvi]	High sensitivity	N	–	2.5	–	–	2.5	–	mVrms
	Low sensitivity		–	1.5	–	–	1.5	–	
Saturation output voltage		Vsat	2.8	–	–	2.8	–	–	V

[xii] Video output is negative-going output with respect to the output offset voltage.
[xiii] Difference between output reference voltage and absolute output voltage with an integration time of 25 ms.
[xiv] Measured with tube energy of 50KVp. Other scintillations with different sensitivity are available.
[xv] Measured without scintillation. When the photodiode array is exposed to uniform light which is 50% of the saturation exposure, the Photo Response Non Uniformity (PRNU) is defined as follows:

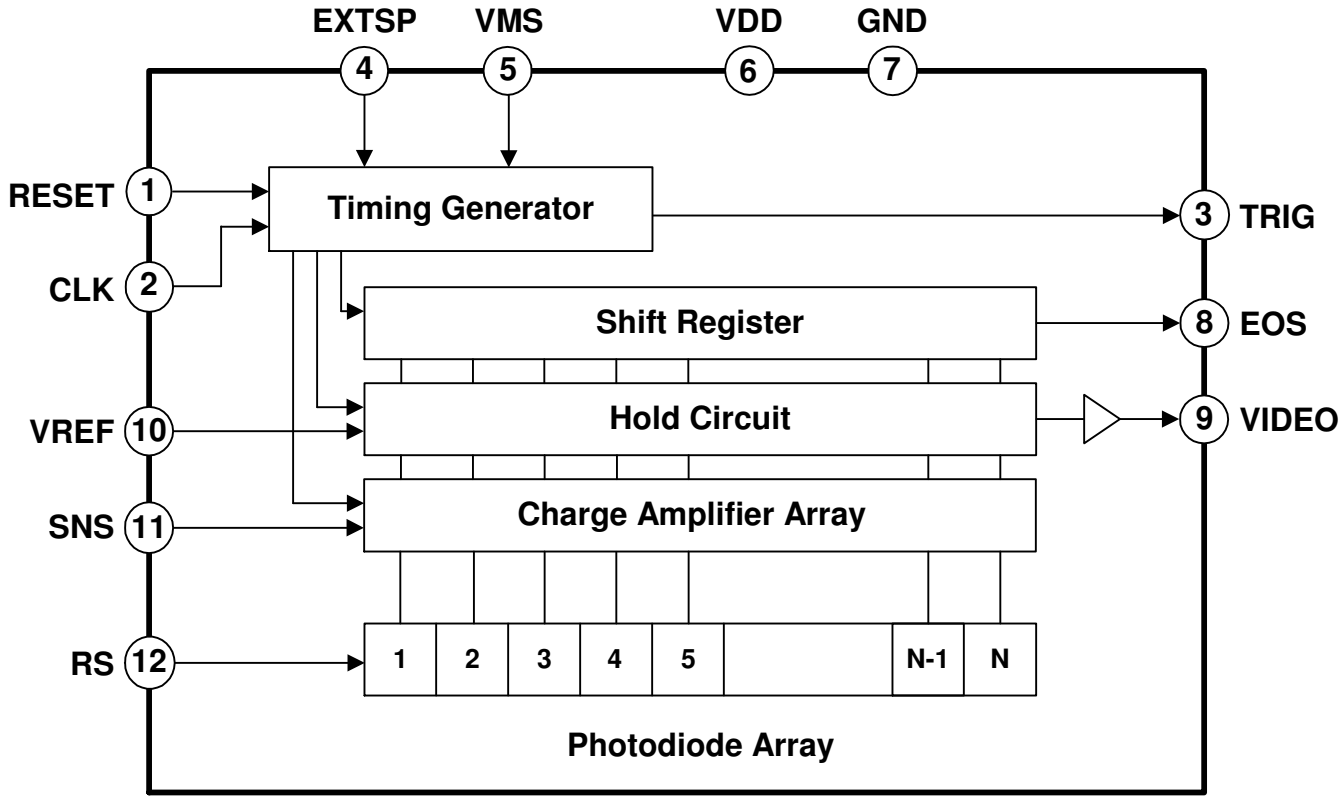
$$PRNU = \Delta X \div X \times 100\%$$

where X is the average output of all elements and ΔX is the difference between the maximum and minimum outputs.
[xvi] Measured with a video data rate of 750 KHz and an integration time of 25 ms in dark state.

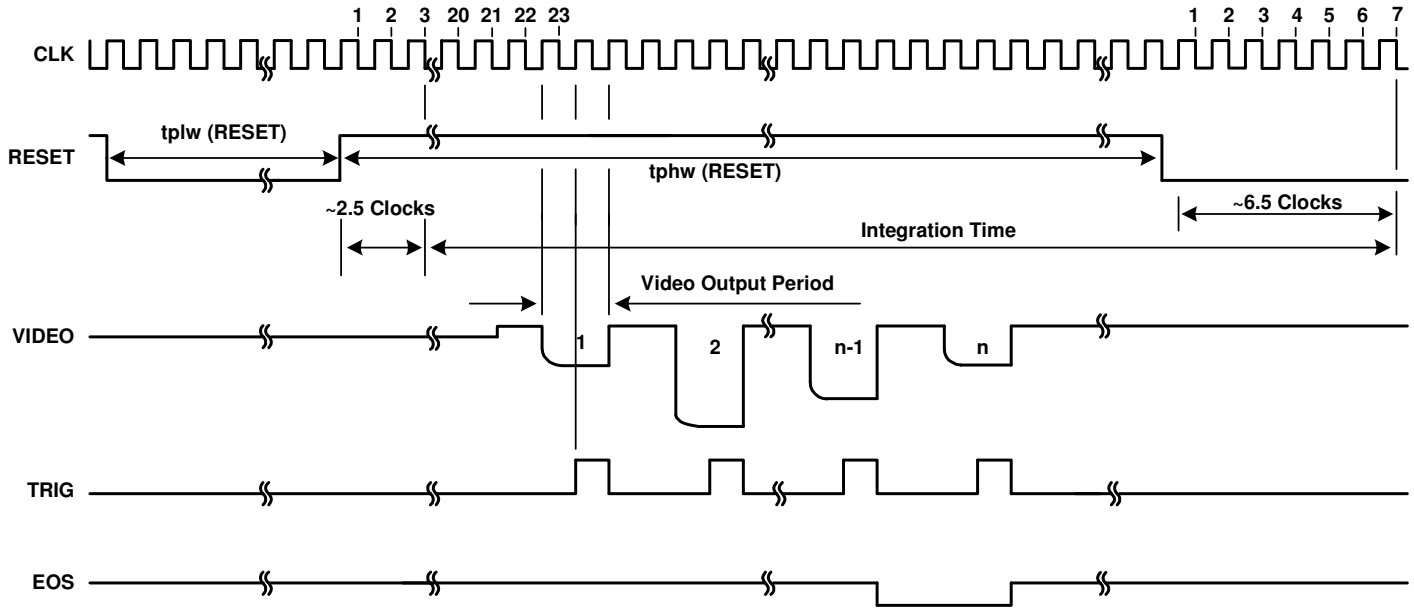
■ **Output waveform of one element**

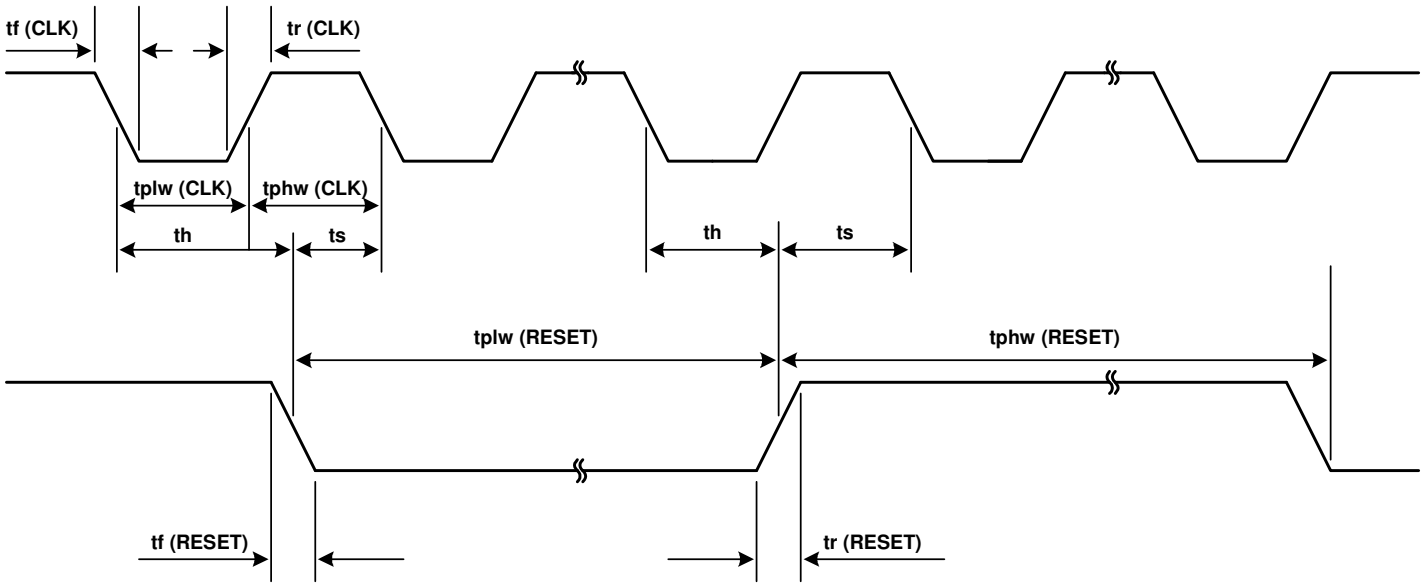


■ **Block diagram**



■ **Timing chart**[xvii]





Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse low/high width	tplw (CLK), tphw (CLK)	100	–	–	ns
Clock pulse rise/fall times	tr (CLK), tf (CLK)	0	20	30	ns
Reset pulse low width[xviii]	tplw (RESET)	12/ f(CLK)	16 / f(CLK)	–	ms
Reset pulse high width[xix]	tphw (RESET)	20	–	–	µs
Reset pulse rise/fall times	tr (RESET), tf (RESET)	0	20	30	ns
Reset pulse setup time[xx]	ts	40	–	–	ns
Reset pulse hold time	th	40	–	–	ns

[xvii] The falling of Video just before the 23th falling edge of CLK after transition of RESET from Low to High corresponds to the first pixel. The video output for the first pixel should be read around the 24th falling edge and before the subsequent rising CLK edge while Trig is high. After the first pixel, a pixel output appears on Video at every 4th clock cycle.

Care should be taken to prevent the rising edge of the RESET during the video output. Improper positioning of the RESET edges can lead to interference with the read-out.

The falling edge of the RESET should follow the last pixel of the previous line's read-out. Thus, one cycle of RESET pulses cannot be set shorter than the time equal to (34 + 4 × N) clock cycles, where N is the number of pixels.

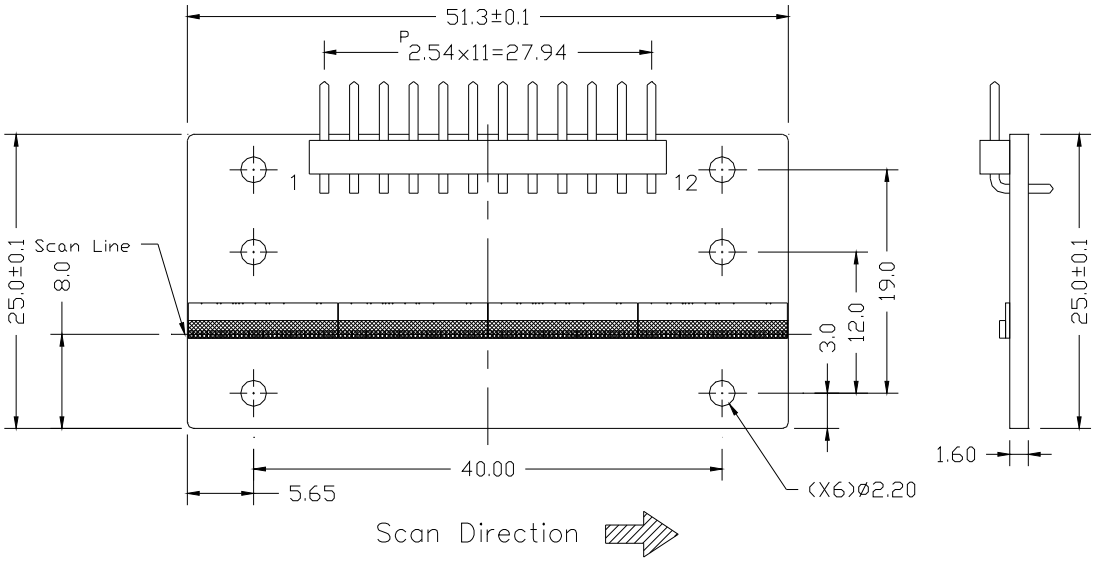
EOS of each detector chip appears during the output of the last pixel.

[xviii] RESET must stay Low [tplw(RESET)] for at least twelve clock cycles; the low pulse width tplw(RESET) should be an integer multiple of four clock cycles [4/f(CLK)].

[xix] The falling edge of RESET pulse determines the end of the integration time, while the rising edge of the RESET pulse determines the start of the integration time and the start of signal read-out. As a result, the signal-charge integration time can be controlled externally with the width of the RESET pulse [tphw(RESET)]. However, the charge integration does not start at the rise of a RESET pulse but starts at the 2nd falling edge of clock after the rise of the RESET pulse and ends at the 7th falling edge of clock after the fall of the RESET pulse.

[xx] The rising and falling edges of RESET must observe the setup and hold time requirements around the falling edges of CLK.

■ Mechanical drawings[xxi]



[xxi] Unit: Dimensions are in millimeters (mm).
Board: FR4 epoxy resin bonded glass fabric.
Connector: BISON Advanced Technology Corp., Ltd. (www.bison-protech.com), P101-RGP-060/030-12 or similar.

■ Pin connections

Pin No.	Symbol	Name	Description
1	RESET	Reset Pulse	Negative-going pulse input
2	CLK	Clock Pulse	Pulse input
3	TRIG	Trigger Pulse	Positive-going pulse output
4	EXTSP	External Start Pulse	Pulse/voltage input
5	VMS	Master/Slave Selection Voltage	Voltage input: See Master/slave selection voltage VMS and external start pulse EXTSP settings note
6	VDD	Supply Voltage	5-V supply voltage
7	GND	Ground	Common ground voltage
8	EOS	End of Scan	Negative-going pulse output
9	VIDEO	Video Output	Negative-going output with respect to VREF
10	VREF	Reference Voltage	Voltage input
11	SNS	Sensitivity Selection	Voltage input: High (VDD) for high sensitivity (Cfhs) Low (GND) for low sensitivity (Cfls)
12	RS	Resolution Selection	Voltage input: High (VDD) for 50-um pitch Low (GND) for 100-um pitch

■ **Master/slave selection voltage VMS and external start pulse EXTSP settings**

For most applications, multiple detectors are read out in parallel. To ensure parallel read out, set the VMS input of all detectors to VDD (A in the table below).

In applications where two or more linearly connected detectors are read out sequentially (in series), set the VMS input of the first detector to VDD and the VMS input of each subsequent (second and later) detector to GND while connecting the EXTSP input of each subsequent detector to the EOS output of each respective preceding detector (B in the table below). The CLK and RESET pulses should be shared among all detectors and the Video output terminals of all detectors are connected together. The maximum number of detectors that can be daisy-chained together is limited by the maximum Video output capacitance requirement.

	Operation Mode	VMS	EXTSP
A	Master configuration: Parallel readout: all detectors Serial readout: 1st detector only	VDD	Don't care
B	Slave configuration: Serial readout: 2nd and later detectors	GND	Preceding detector's EOS should be input

■ **Readout circuit**

In order to minimize noise and to maximize performance, an operational amplifier should be placed as close to the detector to amplify the Video signal.

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